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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/971,981	10/04/2001	Igor Y. Khandros	P64C1-US	5620

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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/971,981	KHANDROS ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *47-66* is/are allowed.

6)☒ Claim(s) *67 and 69-71* is/are rejected.

7)☒ Claim(s) *68* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Rejections Based On Prior Art

1. The following references were relied upon for the rejections hereinbelow:

Chang et al. (US 6,168,974 B1) Reddy (US 6,403,448 B1)

Tatematsu (US 5,138,419)

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 67 and 69-71 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al.

As to Claim 67, Chang et al. discloses, in Fig. 5A: an unsingulated semiconductor wafer comprising a plurality of dice 532 and 534; circuit element means 540 for affecting an electrical signal, the circuit element means 540 attached to and overlapping at least two dice 532 and 534 (col.25: 57-col.26: 11; col.26: 29-33).

As to Claim 69, Chang et al. further discloses a plurality of circuit element means 540 corresponding to the *plurality* (col.25: 57-60) of dice, of which dice 532 and 534 are only two (col.25: 57-67).

As to Claim 70, Chang et al. further discloses electrical connection means (bond wires 558, 550 and bond pads 554, 556) for attaching the circuit element means 540 to the at least two dice 532, 534 (Fig. 5A).

As to Claim 71, Chang et al. further discloses that the semiconductor wafer further comprises scribe lanes 570 between dice 532 and 534, and circuit element means 540 overlaps at least one of the scribe lanes (col.25: 62-65; col.26: 29-33).

4. Claims 67 and 69-71 are rejected under 35 U.S.C. 102(e) as being anticipated by Reddy.

As to Claim 67, Reddy discloses, in Figs. 2a,b,c, 4 and 5: an unsingulated semiconductor wafer 12 comprising a plurality of dice 10; circuit element means 14 for affecting an electrical signal, the circuit element means 14 attached to and overlapping at least two dice 10 (see Figs. 2a, 3 and 4; col.4: 43-46).

As to Claim 69, Reddy further discloses a plurality of circuit element means 14 (Fig. 2a).

As to Claim 70, Reddy further discloses electrical connection means for attaching circuit element means to the at least two dice 10 (Figs. 4 and 5; col.5: 54-col.6: 3).

As to Claim 71, Reddy further discloses the semiconductor wafer 12 comprises scribe lanes 16 between dice 10, and circuit element means 14 overlaps at least one of the scribe lanes 16 (Fig. 2a; col.4: 11-16).

5. Claims 67 and 69-71 are rejected under 35 U.S.C. 102(b) as being anticipated by Tatematsu.

As to Claim 67, Tatematsu discloses, in Fig. 2: an unsingulated semiconductor wafer 1 comprising a plurality of dice 2; circuit element means 4 (bond wires) for affecting an electrical signal (col.4: 3-8), the circuit element means 4 attached to and overlapping at least two dice 2 (Fig. 8: see dice 2R1 and 2D with bonding pads 7 connected by bonding wires 4).

As to Claim 69, Tatematsu further discloses a plurality of circuit element means 4 (Fig. 2).

As to Claim 70, Tatematsu further discloses electrical connection means (bonding pads on the dice) for attaching the circuit element means 4 to the at least two dice 2 (col.4: 6-11).

As to Claim 71, Tatematsu further discloses that semiconductor wafer 1 further comprises horizontal scribe lanes 8 (see Fig. 9) between dice 2 (compare Figs. 8 and 9), the circuit element means 4 overlaps at least one of the horizontal scribe lanes 8 (Fig. 8).

Allowable Subject Matter

6. Claims 47-66 have been allowed.

7. Claim 68 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 47-56, patentability resides in *attaching an electronic component to at least two dice of an unsingulated semiconductor wafer, the electronic component overlapping the at least two dice*, in combination with the other limitations of base Claim 47.

As to Claims 57-66, patentability resides in *an electronic component attached to and overlapping at least two dice of an unsingulated semiconductor wafer*, in combination with the other limitations of base Claim 57.

As to Claim 68, patentability resides in the limitation wherein *a first portion of the circuit element means that overlaps one of the at least two dice* ***differs*** *from a second portion of the circuit element means that overlaps another of the at least two dice*, in combination with the other limitations of the claim.

9. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) The following references disclose an electronic component (a chip) overlapping other chips, but the other chips are not part of an **unsingulated** semiconductor wafer:

Tower (US 4,467,342): Fig. 4b.

Rostoker (US 5,399,898): Fig. 4a.

Pasch (US 5,489,804): Fig. 15b (col.26: 22-31).

b) Mori et al. (US 6,287,949 B1) discloses an unsingulated semiconductor wafer comprising chip units 32 interconnected by circuit elements 37 overlapping at least two chip units 32 (Fig. 5C).

c) Oki et al. (US 5,605,844) discloses an unsingulated semiconductor wafer 10 comprising dice 10a electrically interconnected by an overlapping circuit element; i.e., a contactor 15 having probe contacts that are connected to the test electrodes of dice 10a (Figs 1b,c; bumps 13; col.9: 65-col.10: 2).

d) Degani et al. (US 6,077,725) discloses circuit board patterns 103 and 104 for receiving a plurality of chips of an unsingulated wafer in order to enhance the circuit functionality (Fig. 10; col.7: 52-56).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
December 15, 2002